ECE6332 Project Proposal: Near-Threshold Performance Variations in Future Technology Nodes with PTM

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1 Problem Statement

Due to limited scaling of supply voltage, the power density of a processor is increasing across technology nodes recently. Therefore, the energy efficiency is becoming one of the most significant design constraints for modern processors. Near-threshold computing (NTC), which aggressively the supply voltage close to the circuit's threshold voltage, has exhibited its promising potential in improving energy efficiency. By lowering supply voltage from a nominal 1.1 V to 400-500 mV, Dreslinski et al. has reported energy efficiency gains up to 10x in [1]. However, there are a couple of critical issues associated with NTC, one of which, for example, is the performance variation. With supply voltage close to the threshold, the switching speed of a circuit is more sensitive to variations in threshold voltage. According to [1], global process variation, along with temperature and supply ripple, increases the performance uncertainty of a circuit up to 20x when reduce supply voltage from the nominal 1 V to 0.4 V with existing technology process. As one of alternatives to improve energy efficiency for future processor design, NTC's sensitivity in performance variation with future technology nodes is an essential research problem to be pursued.

My project proposes studies on performance variations of near-threshold circuit with future technology nodes. The studied circuit comes from a critical path of ALU in OpenRISC [2]. This circuit is synthesized with Nangate Open Cell library for 45nm. The generated netlist of the circuit is simulated with PTM [3]. This project aims at technology nodes from 45nm down to 16nm. Propagation delay is the primary metrics for the performance in this project. The project is proposed to study two aspects of the delay for a given technology node. Firstly, assuming no variations in threshold and any other parameters, observe how delay changes with supply voltage sweeping from nominal voltage down to threshold. Secondly, taking global process variation into consideration, observe delay variation with a given supply voltage related to threshold variation using Monte Carlo simulation. These studies are applied to all future technology nodes mentioned before.

2 Novelty

The proposed project is novel mainly in its predictive study of performance variation with future technology node. Since performance degradation is one of the most significant issues preventing NTC to be widely used as a solution to general computing. Although techniques, such as cluster based architecture, are effective to compensate for the performance loss of lower supply with parallelization, performance variations exacerbate the worst performance of a cluster and exert further challenge for performance improvement with NTC. As a result, the conclusion of this project is vital for evaluating the effectiveness of NTC-based cluster architecture designs with future technology nodes.

3 Outcomes

The outcomes of this project are expected to include the circuit delay characterization related to supply voltage, as well as delay variation study related to global process variation. Both results are presented for

various technology nodes.

4 Preliminary Results

As to the date of this proposal, I have obtained a couple of preliminary results.

4.1 Circuit Design

The circuit of the ALU is synthesized with Nangate Open Cell Library, the schematic of the circuit is shown in Figure 1.

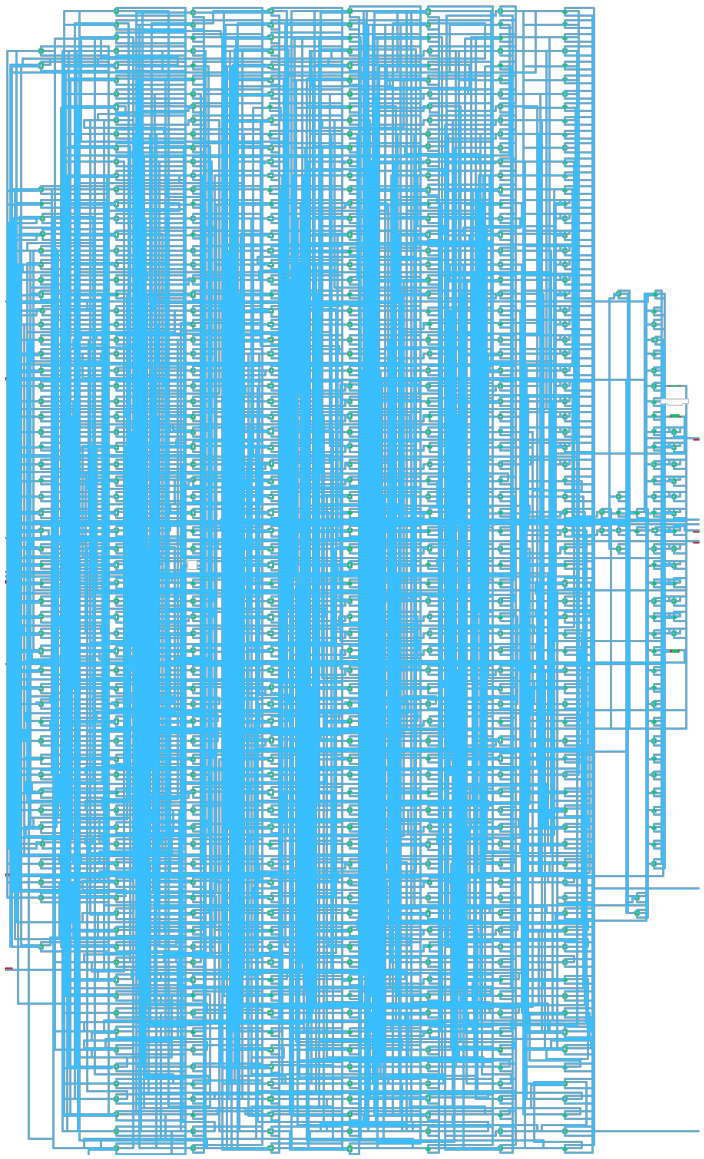
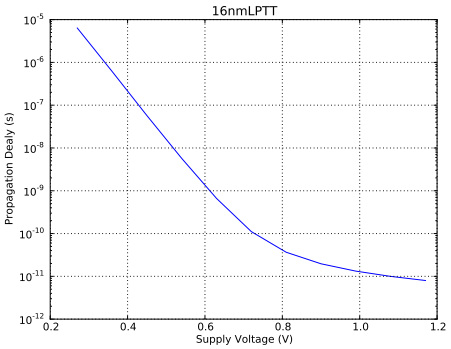
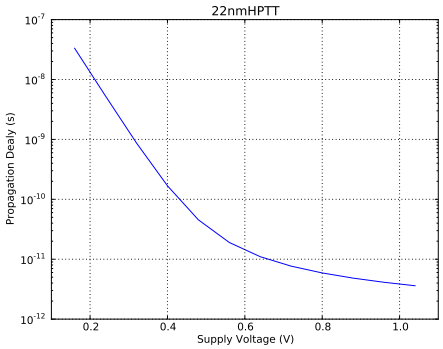


Figure 1: Schematic of ALU in OpenRISC.

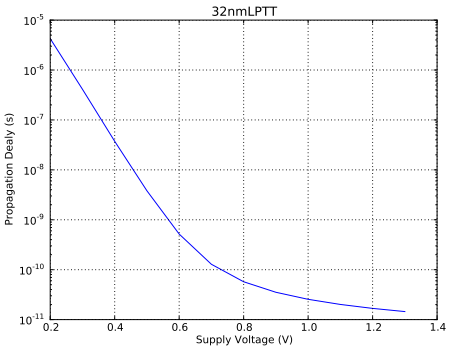
4.2 Inverter Simulation



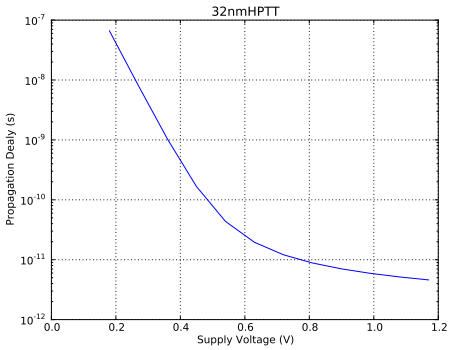
(a) 16nm low power with corner case of 'TT'



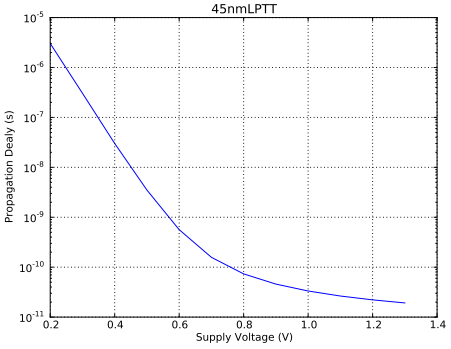
(b) 22nm high performance with corner case of 'TT'



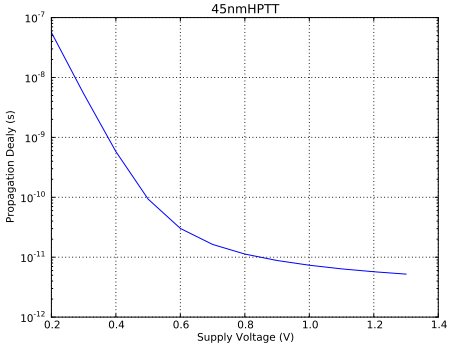
(c) 32nm low power with corner case of 'TT'



(d) 32nm high performance with corner case of 'TT'



(e) 45nm low power with corner case of 'TT'



(f) 45nm high performance with corner case of 'TT'

References

[1] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," *Proceedings of the IEEE, Special Issue on Ultra-Low Power Circuit Technology*, vol. 98, pp. 253–266, February 2010.

[2] M. Erlandsson, M. Unneback, and J. Baxter, "OR1200 OpenRISC processor." http://opencores.org/openrisc,or1200.

[3] Nanoscale Integration and Modeling (NIMO) Group, "Predictive Technology Model (PTM)." http://ptm.asu.edu.